clamp means is connected to said fourth port of said voltage inverter, said connections of bulk and drain of said PMOS device are commonly connected to said first port of said ESD pulse clamp means, said connection of source of said PMOS device is connected to said second port of said ESD pulse clamp means, said connection of gate said PMOS device is connected to said third port of said ESD pulse clamp means.

REMARKS

Examiner Isabel Rodriguez is thanked for thoroughly reviewing the instant application and for examining the Prior Art.

Examiner is also thanked for the indication of allowing claims 21 and 23-28. Examiner is further thanked for the indication of allowing claims 12, 14-19 if these claims are rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Favorable reconsideration of this application in light of the above amendments and the following remarks is respectfully requested.

A new ESD (Electrostatic Discharge) protection circuit with well-triggered PMOS is provided for application in power-rail ESD protection. A PMOS device is connected between the VDD and VSS power lines to sustain the ESD overstress current during the time that the ESD voltage is applied between the VDD and the VSS power lines. In deep submicron CMOS p-substrate technology, the weak point of ESD overstress control is typically associated with the NMOS device. For this reason, the invention uses a power-rail ESD clamp circuit that incorporates a PMOS device. Applying gate-coupled and N-well triggering techniques, the PMOS can be turned on more efficiently when the ESD overstress is present between the power lines. For p-substrate CMOS technology, it is difficult to couple a high voltage to the substrate of the NMOS device while high voltage is readily coupled to the N-well of a PMOS device. The proposed ESD clamp circuit can be applied efficiently to protect the ESD overstress between power rails.

The invention more specifically provides for:

- an ESD pulse detection circuit that triggers the well of a PMOS device for efficient turn-on of the ESD clamp circuit under conditions of ESD overstress, and
- an ESD pulse detection circuit that efficiently triggers the lateral p-n-p parasitic junction transistor and the vertical

p-n-p parasitic junction transistor under conditions of ESD overstress.

Claim rejections - 35 U.S.C. § 102

Reconsideration of the rejection of claims 1-9 and 12 under 35 U.S.C 102(b) as being anticipated by Ker (IEEE Transactions on Electron Devices, Vol. 46, No. 1, January '99) is respectfully requested based on the following.

One of the significant differences between Ker and the instant invention is that, as shown in Fig. 6 of Ker, the ESD clamp circuit comprises a NNOS device, a described in the text under II, Efficient VDD-To-VSS ESD Clamp Circuit, the first sentence.

Kerr therefore does not make use of, as stated above, an ESD pulse detection circuit that triggers the well of a PMOS device for efficient turn-on of the ESD clamp circuit under conditions of ESD overstress.

Ker further does not make use of an ESD pulse detection circuit that efficiently triggers the lateral p-n-p parasitic junction transistor and the vertical p-n-p parasitic junction transistor under conditions of ESD overstress.

The issue of providing an ESD protection circuit that is addressed by the instant invention has been described in detail in the specification, from which is quoted to following:

"In deep submicron CMOS p-substrate technology, the weak point of ESD overstress control is typically associated with the NMOS device. For this reason, the invention uses a power-rail ESD clamp circuit that incorporates a PMOS device. Applying gate-coupled and N-well triggering techniques, the PMOS can be turned on more efficiently when the ESD overstress is present between the power lines. For p-substrate CMOS technology, it is difficult to couple a high voltage to the substrate of the NMOS device while high voltage is readily coupled to the N-well of a PMOS device. The proposed ESD clamp circuit can be applied efficiently to protect the ESD overstress between power rails."

Claims 1 and 10 have been amended in order to incorporate the specific use of a PMOS device in the ESD clamp circuit of the invention. The amendment that has been made to claim 1 has been derived from existing claim 10 and does therefore not introduce new matter.

Since all the claims within this rejection are dependent upon amended claim 1 and carry all of the limitations of amended

claim 1, applicant additionally asserts that those remaining claims may not also properly be rejected under 35 U.S.C 102(b) as being anticipated by Ker, for reasons cited by the examiner.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejection of claims 1-9 and 12 under 35 U.S.C 102(b) as being anticipated by Ker, be withdrawn.

Claim rejections - 35 U.S.C. § 103

Reconsideration of the rejection of claims 10-11 and 20 under 35 U.S.C 103(a) as being unpatentable over Ker (IEEE Transactions on Electron Devices, Vol. 46, No. 1, January '99) in view of Lien (U.S. Patent 5,086,365) is respectfully requested based on the following.

Claims 1 and 10 have been amended in order to incorporate the specific use of a PMOS device in the ESD clamp circuit of the invention. The amendment that has been made to claim 1 has been derived from existing claim 10 and does therefore not introduce new matter.

Furthermore, since claim 10 within this rejection is dependent upon amended claim 1 and carries all of the

limitations of amended claim 1 while claim 11 is dependent on claim 10, applicant additionally asserts that claims 10 and 11 may not also properly be rejected under 35 U.S.C 102(b) as being anticipated by Ker, for reasons cited by the examiner.

Claim 20 has been amended by specifying that the ESD clamp circuit of the invention comprises a PMOS device. This specification has previously been provided in existing claim 10 and does therefore not introduce new matter.

The amended claim 20 makes claim 20 different from the Ker invention while it can further be stated that the instant invention differs from the Lien invention since the Lien invention does not make use of the main aspects of the instant invention, as highlighted above, that is the Lien invention does not provide:

- an ESD pulse detection circuit that triggers the well of a PMOS device for efficient turn-on of the ESD clamp circuit under conditions of ESD overstress, and
- an ESD pulse detection circuit that efficiently triggers the lateral p-n-p parasitic junction transistor and the vertical p-n-p parasitic junction transistor under conditions of ESD overstress.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejection of claims 10-11 and 20 under 35 U.S.C 103(a), be withdrawn.

Claim rejections - 35 U.S.C. § 103

Reconsideration of the rejection of claim 13 under 35 U.S.C 103(a) as being unpatentable over Ker et al. (IEEE Transactions on Electron Devices, Vol. 46, No. 1, January '99) in view of Mead (Introduction to VLSI Systems) is respectfully requested based on the following.

Claim 1 has been amended in order to incorporate the specific use of a PMOS device in the ESD clamp circuit of the invention. The amendment that has been made to claim 1 has been derived from existing claim 10 and does therefore not introduce new matter.

Since claim 13 within this rejection is dependent upon amended claim 1 and carries all of the limitations of amended claim 1, applicant additionally asserts that claim 13 may not also properly be rejected under 35 U.S.C 102(b) as being anticipated by Ker, for reasons cited by the examiner.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejection of claim 13 under 35 U.S.C 103(a), be withdrawn.

Claim rejections - 35 U.S.C. § 103

Reconsideration of the rejection of claim 22 under 35 U.S.C 103(a) as being unpatentable over Ker (IEEE Transactions on Electron Devices, Vol. 46, No. 1, January '99) in view of Mead and further in view of Lien (U.S. Patent 5,086,365) is respectfully requested based on the following.

Claim 22 has been amended by specifying that the ESD clamp circuit of the invention comprises a PMOS device. This specification has previously been provided in existing claim 10 and does therefore not introduce new matter.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejection of claim 22 under 35 U.S.C 103(a), be withdrawn.

Other Considerations

No new independent or dependent claims have been written as a result of this office action, no new charges are therefore incurred due to this office action.

SUMMARY

A new ESD (Electrostatic Discharge) protection circuit with well-triggered PMOS is provided for application in power-rail ESD protection. A PMOS device is connected between the VDD and VSS power lines to sustain the ESD overstress current during the time that the ESD voltage is applied between the VDD and the VSS power lines. In deep submicron CMOS p-substrate technology, the weak point of ESD overstress control is typically associated with the NMOS device. For this reason, the invention uses a power-rail ESD clamp circuit that incorporates a PMOS device. Applying gate-coupled and N-well triggering techniques, the PMOS can be turned on more efficiently when the ESD overstress is present between the power lines. For p-substrate CMOS technology, it is difficult to couple a high voltage to the substrate of the NMOS device while high voltage is readily coupled to the N-well of a PMOS device. The proposed ESD clamp

circuit can be applied efficiently to protect the ESD overstress between power rails.

It is requested that, should Examiner not find the claims to be allowable, to call the undersigned Attorney at the Examiner's convenience at 845-452-5863 in order to overcome any problems preventing allowance of the claims.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned:

"Version with markings to show changes made."

Respectfully submitted,

Stephen B. Ackerman (Reg. No 37,761)

Version with markings to show changes made

IN THE SPECIFICATION

1) page 1, last paragraph, page 2, first paragraph, please replace this text with the following:

In [the] deep submicron CMOS technology, ESD damage has become one of the main reliability concerns. [Some processing] Processing techniques that [is] are applied in advanced CMOS technology procedures can lead to degradation of the performance of ESD circuits that are part of [the creation of] Integrated Circuits (IC's). Examples of these advanced processing techniques are the formation of Lightly Doped Drain (LDD) regions in the MOSFET devices, the formation of salicided drain/source surface regions for MOSFET devices and the formation of extremely thin gate oxide layers underneath the gate electrodes of MOSFET devices. To improve the performance of ESD circuitry of deep submicron CMOS IC's, a number of design methods and approaches have been proposed and applied to I/O cells and Power/Ground cells of semiconductor devices. These methods [included] include ESD protection devices, ESD protection circuits, ESD layout technique[,] and process modifications.

For general industrial applications, the input/output pins of the Integrated Circuits must be able to sustain extreme voltage levels when in contact with an ESD source in excess of 2000 volts. In order to achieve this objective, ESD protection circuits are placed around the I/O pads of the IC's such that these ESD protection circuits protect the IC's against potential ESD damage. The ESD protection circuits shunt the electrostatic charges that originate in the ESD source away from the IC thereby preventing damage to the IC.

2) page 19, last paragraph, page 20, first paragraph, please replace this text with the following:

The phenomenon described above can be simulated by using circuit simulators. For this purpose the [proposed] ESD protection circuit of the invention, [that] which is shown in Fig. 4, has been designed using a [TSMC 0.25um] 0.25 μm logic salicide process. The simulator that has been used for this purpose is a simulator known as Hspice. The W/L of M_{ESD} in the circuit of the invention [is] has a channel width of 30 [um] μm and a channel length of 0.5 [um] μm for each finger of M_{ESD}. There are a total of 10 fingers for M_{ESD} [with] resulting in a total channel width of 300 [um] μm. The W/L of M_P of the inverter [is] has a channel width of 25 [um] μm and a channel

length of 0.35 [um] μm. The W/L of M_N of the inverter [is] has a channel width of 10 [um] μm and a channel length of 0.35 [um] μm. The value of resistance R is 12 Kohm while the value of the capacitance C is 0.5 pF. Simulations under two different operating conditions are required in order to verify the functioning of the circuit of the invention. The first operating conditions represent the ESD overstress conditions where ESD overstress is between the VDD and VSS power rails. The second operating conditions represent the power-on conditions where a voltage of [3.3V] 3.3 Volts exists between the VDD and VSS power rails.

3) page 20, last paragraph, page 21, first paragraph, please replace this text with the following:

The operation of the proposed ESD protection circuit when ESD voltage exists between the VDD and VSS power rails can be explained as [followed] follows. The ESD overstress voltage with an amplitude of 8 volts and a rise time of 10 nS is applied between the VDD and VSS power rails. Because the junction breakdown voltage of the PMOS device 32 (Fig. 4) is about 9.5V, M_{ESD} must be turned on before conditions of junction breakdown occur. Otherwise, the ESD pulse detection circuit is of no help in triggering (switching on) M_{ESD}, as a consequence, the ESD

level will not be improved. When the voltage at VDD is increased, this voltage is coupled to Ni via capacitor C. After the voltage at Ni is above a threshold voltage of M_N, the NMOS device of the inverter will turn on and clamp the voltage at N to a low voltage level. Under these conditions, the voltage between node N and VDD (Fig. 4), Vgs, [is decreasing] decreases from 0 volts to a negative voltage. Whenever the value of Vgs is less than the threshold voltage of M_{ESD}, M_{ESD} will be turned-on. The threshold voltage of M_{ESD}, which is referred to as Vthp, is about -0.86 volts in the circuit shown in Fig. 4.

IN THE CLAIMS

Please amend the claims as follows.

1. (Amended) An Electrostatic Discharge (ESD) protection circuit that is connected between a first terminal and a second terminal of an Integrated Circuit (IC), whereby said ESD protection circuit has as objective to dissipate an electrostatic pulse that originates from an ESD source that is connected between said first terminal and said second terminal thereby protecting said IC from potential damage that can be caused by exposure of said IC to extreme values of voltage from said ESD source, whereby said ESD protection circuit comprises:

a ESD pulse clamp means comprising a PMOS device for shunting said electrostatic pulse from said IC having a first port that is connected to said first terminal of said IC, a second port that is connected to said second terminal of said IC, and a third port; and

an ESD pulse detection means having a first input port connected to said first terminal of said IC, a second input port connected to said second terminal of said IC, an output port that is connected to said third port of said ESD pulse clamp means, whereby in detecting a presence of said electrostatic pulse said ESD pulse detection means generates a voltage that triggers said ESD pulse clamp means thereby shunting said electrostatic pulse from said IC.

10. (Amended) The circuit of claim 1, [wherein] said ESD pulse clamp means [comprises] comprising a PMOS device having connections of gate electrode, source, drain and bulk, whereby said ESD pulse clamp means contains a first port and a second port and a third port.

20. (Amended) An Electrostatic Discharge (ESD) protection circuit that is connected between a first terminal and a second terminal of an Integrated Circuit (IC), whereby said ESD protection circuit has as objective to dissipate an

electrostatic pulse that originates from an ESD source that is connected between said first terminal and said second terminal thereby protecting said IC from potential damage that can be caused by exposure of said IC to extreme values of voltage from said ESD source, whereby said ESD protection circuit comprises:

an ESD pulse clamp means comprising a PMOS device for shunting said electrostatic pulse from said IC having a first port that is connected to said first terminal of said IC, a second port that is connected to said second terminal of said IC, and a third port;

an ESD pulse detection means having a first input port connected to said first terminal of said IC, a second input port connected to said second terminal of said IC, an output port that is connected to said third port of said ESD pulse clamp means;

said ESD pulse detection means containing a network comprising a resistive component, a capacitive component, and a voltage inverter;

said voltage inverter of said ESD pulse detection means comprising a PMOS device having connections of gate electrode, source, drain and bulk, and a NMOS device having connections of gate electrode, source, drain and bulk, whereby said voltage inverter contains a first port, a second port, a third port, and a fourth port, said first port of said voltage inverter is

connected to said first terminal of said IC, said second port of said voltage inverter is connected to said second terminal of said IC, said connections of gate of said PMOS device and said NMOS device are commonly connected to said third port of said voltage inverter, said connection of bulk and drain of said PMOS device is commonly connected to said first port of said voltage inverter, said connection of source and said connection of bulk of said NMOS device are commonly connected to said second port of said voltage inverter, said connection of source of said PMOS device and said connection of drain of said NMOS device are commonly connected to said fourth port of said voltage inverter;

said capacitive component of said ESD pulse detection means comprising a first terminal and a second terminal, said first terminal of said capacitive component being connected to said first terminal of said IC;

said resistive component of said ESD pulse detection means comprising a first terminal and a second terminal, said second terminal of said resistive component being connected to said second terminal of said IC, and said second terminal of said capacitive component and said first terminal of said resistive component being commonly connected to said third port of said voltage inverter; and

said ESD pulse clamp means comprising a PMOS device having connections of gate electrode, source, drain and bulk, whereby

said ESD pulse clamp means contains a first port and a second port and a third port, said first port of said ESD pulse clamp means is connected to said first terminal of said IC, said second port of said ESD pulse clamp means is connected to said second terminal of said IC, said third port of said ESD pulse clamp means is connected to said fourth port of said voltage inverter, said connections of bulk and drain of said PMOS device are commonly connected to said first port of said ESD pulse clamp means, said connection of source of said PMOS device is connected to said second port of said ESD pulse clamp means, said connection of gate said PMOS device is connected to said third port of said ESD pulse clamp means.

22. (Amended) An Electrostatic Discharge (ESD) protection circuit that is connected between a first terminal and a second terminal of an Integrated Circuit (IC), whereby said ESD protection circuit has as objective to dissipate an electrostatic pulse that originates from an ESD source that is connected between said first terminal and said second terminal thereby protecting said IC from potential damage that can be caused by exposure of said IC to extreme values of voltage from said ESD source, whereby said ESD protection circuit comprises:

an ESD pulse clamp means <u>comprising a PMOS device</u> for shunting said electrostatic pulse from said IC having a first

port that is connected to said first terminal of said IC, a second port that is connected to said second terminal of said IC, and a third port;

an ESD pulse detection means having a first input port connected to said first terminal of said IC, a second input port connected to said second terminal of said IC, an output port that is connected to said third port of said ESD pulse clamp means;

said ESD pulse detection means containing a network comprising a resistive component having a first and a second terminal, a capacitive component having a first and a second terminal, and a voltage inverter;

said voltage inverter of said ESD pulse detection means comprising a PMOS device having connections of gate electrode, source, drain and bulk, and a NMOS device having connections of gate electrode, source, drain and bulk, whereby said voltage inverter contains a first port, a second port, a third port, and a fourth port, said first port of said voltage inverter is connected to said first terminal of said IC, said second port of said voltage inverter is connected to said second terminal of said IC, said connections of gate of said PMOS device and said NMOS device are commonly connected to said third port of said voltage inverter, said connections of bulk and drain of said PMOS device are commonly connected to said first port of said

voltage inverter, said connection of source and said connection of bulk of said NMOS device are commonly connected to said second port of said voltage inverter, said connection of source of said PMOS device and said connection of drain of said NMOS device are commonly connected to said fourth port of said voltage inverter;

said capacitive component of said ESD pulse detection means comprises a PMOS device having connections of gate electrode, source, drain and bulk whereby said connections of source, drain and bulk of said PMOS device are commonly connected to said first terminal of said capacitive component, said connection of gate is connected to said second terminal of said capacitive component.

said resistive component of said ESD pulse detection means comprising a first terminal and a second terminal, said second terminal of said resistive component being connected to said second terminal of said IC, and said second terminal of said capacitive component and said first terminal of said resistive component being commonly connected to said third port of said voltage inverter; and

said ESD pulse clamp means comprising a PMOS device having connections of gate electrode, source, drain and bulk, whereby said ESD pulse clamp means contains a first port and a second port and a third port, said first port of said ESD pulse clamp

means is connected to said first terminal of said IC, said second port of said ESD pulse clamp means is connected to said second terminal of said IC, said third port of said ESD pulse clamp means is connected to said fourth port of said voltage inverter, said connections of bulk and drain of said PMOS device are commonly connected to said first port of said ESD pulse clamp means, said connection of source of said PMOS device is connected to said second port of said ESD pulse clamp means, said connection of gate said PMOS device is connected to said third port of said ESD pulse clamp means.